UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/239,907	01/29/1999	ANDREW MACCORMACK	858063.435	6683
SEED INTELLECTUAL PROPERTY LAW GROUP PLLC 701 FIFTH AVE SUITE 5400 SEATTLE, WA 98104			EXAMINER	
			PENG, FRED H	
			ART UNIT	PAPER NUMBER
			2426	
			MAIL DATE	DELIVERY MODE
			10/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte ANDREW MacCORMACK, HOWARD GURNEY, WILLIAM ROBBINS, and FABRIZIO ROVATI

Appeal 2008-3215 Application 09/239,907 Technology Center 2600

Decided: October 31, 2008

.____

Before KENNETH W. HAIRSTON, MAHSHID D. SAADAT and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, Administrative Patent Judge.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from non-final rejections of claims 1, 3-11, 13-42, 45, and 46. Claims 43 and 44 have been indicated to be allowable if rewritten in independent form. (*See* App. Br. 2). No other claims are pending. (*See* Office Action, mailed February 8, 2006). We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Appellants' claimed invention relates to demultiplexing of a digital data stream. The data stream contains packets, each of which has a header containing a packet identifier (PID) which identifies the type of packet: either 1) packetized elementary stream (PES - audio, video, or private), or 2) program specific information (PSI). (*See* generally Spec. 1-3, filed March 10, 2003). A receiver parses the packets for the desired payload data (PES or PSI) in the packet by matching stored PIDs in a table with incoming PIDs in the packet headers. The headers are not scrambled, but the payloads might be. (*See* Spec. 6-8). If the stored and incoming PIDs match, a search engine retrieves a pointer stored with a particular PID to point to descrambling keys or other control information for use by an input module for descrambling/controlling the payloads. (Spec. 10).

The Examiner relies on the following prior art references:

Bestler	5,602,920	Feb. 11, 1997
Blatter	5,844,595	Dec. 1, 1998
Dokic	5,959,659	Sept. 28, 1999

ADSP-2100 Family User's Manual 3rd Edition (9/95) – Chapter 4: Data Transfer (*hereinafter* "User's Manual").

Claims 1 and 3-10 stand rejected under 35 U.S.C.

§ 112 as failing to comply with the written description requirement.

Claims 39-41, 45, and 46 stand rejected under 35 U.S.C.

§ 102(e) as being anticipated by Dokic.

Claims 11 and 13-20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the collective teachings of Dokic and the User's Manual.

Claims 21-38 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the collective teachings of Dokic and Blatter.

Claim 42 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the collective teachings of Dokic and Bestler.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Brief (filed June 4, 2007), the Reply Brief (filed December 17, 2007), and the Answer (mailed October 17, 2007) for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073-74 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41 (2007). Such a showing requires:

'some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness'. . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id., 127 S. Ct. at 1741 (*quoting In re Kahn*, 441 F.3d 977, 987 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

We note that the patent drafter is in the best position to resolve the ambiguity in the patent claims, and it is highly desirable that patent examiners demand that applicants do so in appropriate circumstances so that the patent can be amended during prosecution rather than attempting to resolve the ambiguity in litigation.

Halliburton Energy Services, Inc. v. M-I LLC, 514 F.3d 1244, 1255 (Fed. Circ. 2008). "The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed." In re Zletz, 893 F.2d 319, 321 (Fed. Cir. 1990) (holding that the BPAI erred by applying the wrong legal standard of claim interpretation during prosecution versus litigation, where the BPAI read limitations into the claim from the specification) (citations omitted).

ANALYSIS

35 U.S.C. § 112 rejection of Claims 1 and 3-10

With respect to claims 1 and 3-10, Appellants and the Examiner disagree over the final clause in claim 1¹; namely, "wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to *the match signal by the input module*." The disagreement arises because an earlier clause in claim 1 calls for "a third control circuit . . . for setting a match signal" (emphasis added).

Thus, the Examiner contends the last clause contradicts the earlier clause, because, under the Examiner's interpretation, the claim calls for a match signal from both the third control circuit and the input module (Ans. 3-4). Appellants disagree, arguing that the Examiner misreads the last clause, because, according to Appellants, the phrase "controls processing" modifies "input module," while the phrase "responsive to the match signal" modifies "data packet." (App. Br. 17-18). Hence, while the rejection is formally couched in terms of the written description and enablement requirements under 35 U.S.C. 112 1st ¶, the Examiner and Appellants actually disagree over the clarity of the claims, thereby raising 35 U.S.C. 112 2nd ¶ concerns. (*See* Reply to Office Action, p. 20-22, filed April 10, 2006; App. Br. 17-18; Ans. 3-4, 14).

¹ Independent Claim 10 raises the same issues. Claims 3-9 depend from claim 1. Therefore, we select claim 1 as representative of the group.

Claim 1 reads as follows:

1. A receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

an input module for receiving and processing the digital data stream;

a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;

a first control circuit for controlling the storage in the memory of the packet identifiers;

a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and

a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

We find that under Appellants' interpretation as outlined *supra*, claim 1 is supported by the disclosure. Under the Examiner's, it is not. While Appellants maintains the claim is clear, Appellants' proffered an amendment "to eliminate any possible ambiguity." (Reply to Office Action, *supra*, p. 21).²

² The Examiner cited new issue concerns and refused to enter the amendment (After Final Office Action, mailed April 26, 2006).

We determine that the claim is ambiguous because one can read it at least either of the two ways delineated in the arguments by the Examiner and Appellants.³ In light of our finding, and Appellants' proffered amendments, we will sustain the Examiner's rejection, *pro forma*. *Haliburton* and *Zletz supra* support our decision by encouraging Examiners to demand clarity and resolve ambiguities during prosecution (to avoid later litigation disputes). Accordingly, we will sustain the Examiner's rejection of claims 1 and 3-10.

35 U.S.C. § 102 rejection of 39-41, 45 and 46.

Regarding this anticipatory rejection, Appellants' arguments are directed to two separate groups of claims: 1) 39-41, and 2) 45, 46. (App. Br. 18-20). Regarding claims 45-46, Appellants rely on arguments presented for claim 39; however, claim 45 differs in scope from claim 39. Accordingly, we select claims 39 and 45 as respectively representative of the two groups of claims.

Claim 39 reads as follows:

39. A receiver for processing a packetized digital data stream, the receiver comprising:

an input module to receive and process a data packet; a memory;

a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and

³ Entry of Appellants' proffered amendment noted *supra* would vitiate our 35 U.S.C. § 112 concerns.

a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information.

Findings of Fact - Dokic

- 1. Dokic's digital signal processor 102 (DSP) includes transport buffers 200, 202 in the path of an incoming transport stream of MPEG-2 data. Within the transport buffers, the data is "parsed, interpreted, and transferred to an appropriate buffer" 206, 208 or 210 (col. 8, ll. 15-19) by a controller 204 in the DSP. (Col. 7, l. 60 to col. 8, l. 19; Figs. 3, 5).
- 2. The transport stream includes a 4 byte header which includes a packet identifier (PID) identifying the type of data in the payload of a data packet that follows the header. (Col. 1, Il. 48-53).
- 3. The DSP uses one of two sources to demultiplex the transport stream 1) a PID filtering table entered into memory 205 from the host processor 106 or 2) a default program selected by the DSP, in which case, the DSP recovers from the transport stream a program association table (PAT) and a program map table (PMT), which also are loaded into the memory 205. The PMT specifies the PIDs for each of the elementary streams (audio, video or private) in the payload associated with the program. (Col. 2, 11. 3-44, col. 8, 11. 20-67; Figs. 3, 5).

- 4. A host processor 106 loads the PID filtering table into a memory 205 (Fig. 3, col. 8, ll. 26-28). "The PID filtering table is a table of filtering values generated by the host microprocessor that correspond to a user selected program to be decoded from the transport stream." (Col. 8, ll. 28-31).
- 5. The filtering table contains 16 values, "[t]he first two entries within the table identify the PIDs of the transport packets carrying video and audio data, respectively" of the desired program selected. The payloads in the video and audio packets are demultiplexed from the program stream and provided respectively to the video 206 and audio 208 buffers. (Col. 8, Il. 31-36, Fig. 5).
- 6. "The third entry provides the PID of the transport packets that contain program clock reference values." Such values are used by a clock recovery system to recover an encoder clock for system operation. (Col. 8, ll. 37-40).
- 7. Unmatched parsed PIDs in the transport stream are discarded. Parsed PIDs from the transport stream matching the final thirteen table values are sent to the private data buffer 210. (Col. 8, ll. 37-52).
- 8. If the user has not selected a program, or the host processor has not supplied a PID table, the digital signal processor (DSP) 102 defaults to a program selected from a program association table recovered from the transport stream. (See FF 3). The DSP also selects a PMT from the stream and uses the PIDs of the default program therein to demultiplex the stream

for the default video and audio packets of the default program (col. 8, ll. 53-67). Upon a match between the desired and default PIDs, similar to the non-default situation (*see* FF 1-7), the DSP transfers the data to the video buffer 206, audio buffer 208, or the private data buffer 210. If no match occurs, the data is discarded. (Col. 8, ll. 64-67).

Claims 39-41

Appellants dispute the Examiner's determination (Ans. 4-6) that Dokic's host processor 106, cited by the Examiner as the claimed receiver processor, controls storage of "desired packet identifiers *and associated control information* in the memory" 205, as set forth in claim 39. (App. Br. 18-19).

The Examiner generally found that Column 8 of Dokic (*see* Ans. 4-6, 15-17), summarized above (*see* FF 1-8), teaches the disputed control information. The Examiner found that Dokic's PID filter table, the default program, and/or the clock data (*see* FF 1-8) constitute the desired packet identifiers, and the associated control information. Appellants maintain that the claim requires two separate items of information, and that Dokic merely discloses storing the desired packet identifiers (PIDs), but not the associated control information (App. Br. 19).

The Examiner reasoned that the PID filtering table or the PMT containing the desired PIDs, and stored within the memory 205, implicitly contain control information, because upon a match of the PIDs, the DSP

controls the data by sending it either to the audio, video, or private data buffers, or employs the data as clock data (Ans. 15-17).

We generally agree with the Examiner's findings (*see* FF 1-8). We also find that the designated positions of the audio and video slots as first and second address locations in the PID table constitute control information, because a match to those table locations automatically results in the parsed PID data from the transport stream being sent to the correct audio or video data buffers (FF 1-3, 5, 6). That is, the match event *itself* constitutes control information employed by the DSP to control a switch and then send the parsed PID data to the correct buffer 206, 208, 210 (*see* Fig. 5).

However, Appellants further argue that Dokic does not disclose that the control information is retrieved from the memory 205 responsive to the match. (App. Br. 19). We agree with Appellants. The claim requires retrieving such control information from the memory. We find that while Dokic's control occurs responsive to a PID match (*see* FF 1-6), we have no basis for finding that the control information is *retrieved from the memory responsive* to the match, as set forth in the claim, because Dokic implies that such control information is already present as a result of the match at the buffer and/or controller (*see* FF 1, 5, 6, Fig. 5).

That is, we find that processing by the controller 204 occurs in the transport buffers 200, 202 (FF 1, Fig. 5). This implies that the match determination is made at the buffers and/or controller 204, not at the memory 205. While associated control information initially comes from the memory 205 (because the desired video, audio, and private PID locations are

designated in that memory), Dokic does not disclose retrieving any control information from the memory 205 after the match occurs. Rather, Dokic is silent regarding any control information, but as indicated above, we find that Dokic implies that the match occurs in the buffers and/or the controller, and we also infer that any control information emanates from the fact of the match, but whence it comes is simply not disclosed.⁴

While the Examiner also argues that the default program map table (PMT) (*see* FF 3, 8) directs "what PIDs correspond to different data types (audio, video, data) [and] [t]his control information serves as 'control information' because it is used by the receiver [100] to direct a particular PID to the appropriate decoder [120/122] audio or video" (Ans. 16), similar to our analysis above, we find that the PMT helps to *create* a PID match in the buffers, the PMT is not retrieved *as a result* of the match. Similar remarks apply to the clock data – the clock data helps to create a PID match in the buffers.

We also find that as the Examiner argued (Ans. 16-17), and contrary to Appellants' argument (App. Br. 19), Dokic's host microprocessor controls storage of the control PMT/PSD information, because the DSP only creates such default program information when the host microprocessor allows it – i.e., as a default (*see* FF 3, 8).

⁻

⁴ While the buffers constitute memory, the receiver processor 106 does not control the associated control information in the buffer memory as required by claim 39, nor has the Examiner made such a finding.

Accordingly, we will not sustain the Examiner's rejection of claims 39-41.

Claims 45 and 46

Appellants merely recite certain claim limitations for claims 45 and 46, and state that "as discussed above" (i.e., with respect to claim 39), "Dokic does not teach, motivate or suggest retrieving control information associated with a received data packet." (App. Br. 19). Thus, we select claim 45 as representative of this group. Claim 45 is reproduced below:

45. A receiver for processing a packetized digital data stream, the receiver comprising:

means for receiving a data packet in the digital data stream;

means for retrieving control information associated with a received data packet; and

means for controlling processing of a received data packet by the means for receiving a data packet.⁵

The Examiner found that the retrieved control information "could be met either by the stored information that defines the type of PID (audio, video, or data) for directing the PID to the appropriate decoder or information that is subsequently utilized to define the timing information

⁵ Appellants do not argue that the claim falls under 35 U.S.C. 112 6th ¶, nor challenge the Examiner's findings regarding the means plus function limitations recited in the claim. Rather, Appellants argue that Dokic does not disclose a particular function as discussed *infra*. (*See* App. Br. 19-20).

(Dokic: Col. 8, Lines 24-25)." (Ans. 17). We agree with the Examiner. As we found above, Dokic's PID filter table constitutes control information at least by virtue of the respective positions (first, second, etc.) in the table of the stored desired audio, video, data or clock PID data therein (*see* FF 1-8). A match causes the corresponding data payload packet to be sent, via a switch controlled by controller 204 in the DSP (*see* Fig. 5 – unnumbered switch), to the appropriate buffer: video 206, audio 208 or private 210. (*Compare* Ans. 15-17).

Hence, because Dokic's DSP controls a switch based on the match information, the system retrieves a control signal for the switch. Therefore, such control constitutes "means for retrieving control information associated with a received data packet," as recited in claim 45. We emphasize that unlike the situation involved in claim 39, claim 45 does not require the control information to be retrieved from the memory responsive to a match.

As such, we find that the Examiner has at least set forth a sufficient initial showing of anticipation of the claimed invention as recited in independent claim 45. Appellants' arguments do not convince us of error in the Examiner's position. Accordingly, we will sustain the Examiner's rejection of claims 45-46.

35 U.S.C. § 103 rejection of claims 11 and 13-22-Doki with User's Manual

Appellants primarily dispute the Examiner's finding that Dokic's buffers 204, 205 constitute "memory separate from the data stream" as called for in representative independent claims 11 and 20. (App. Br. 21; *see*

also Reply Br. 4). We agree with Appellants. The Examiner's rationale that "the data stream and the memory are distinctive or dissimilar entities in their own rights" (Ans. 18) is not persuasive because it implies that the disputed clause does not further limit the claim. We determine that the term "separate" further limits claim 11, and find that Dokic's buffers 200 and 202 are not separate from, but rather, are in the direct path of the data stream (FF 1, Fig. 5).

The Examiner's supporting rationale that because Appellants' disclosed SRAM 400 is separate from the data stream and stores incoming data, then that fact implies that a memory that stores data from a data stream, such as Dokic's buffer(s), is therefore separate from such data, also is not persuasive (Ans. 17-18). Rather, we find Appellants' argument to be more persuasive: "One of skill in the art would not interpret data buffers in the data stream as a memory that is separate from the data stream, regardless of whether the separate memory might also sometimes store all or part of a data packet." (Reply Br. 4).

Accordingly, for the above reasons, we will not sustain the Examiner's rejection of claims 11 and 20 and claims 13-19 dependent therefrom.

35 U.S.C. § 103 rejection of claims 21-38 - Dokic with Blatter

Appellants traverse the Examiner's finding that Dokic and Blatter collectively teach the first and second data structures as required by independent claims 21 and 29. (App. Br. 23-29). Independent claims 30

and 38 also recite the disputed first and second data structures. Accordingly, we select claim 21 as representative of the group.

Findings of Fact - Blatter

9. Blatter discloses an MPEG decoder/receiver employing PID tables, two data structures, and address pointers:

The PID look-up tables are *memory mapped to encryption key tables* in units 45 and 47 that associate encryption keys with each pre-loaded PID. The memory mapped PID and encryption key look-up tables permit units 45 and 47 to match encrypted packets containing a pre-loaded PID with associated encryption keys that permit their decryption. . . . The PID look-up table in unit 45 is also *memory mapped to a destination* table that matches packets containing pre-loaded PIDs with corresponding destination buffer locations in packet buffer 60. The encryption keys and destination buffer location *addresses* associated with the programs selected by a user for viewing or storage are pre-loaded into units 45 and 47 along with the assigned PIDs by controller 115.

(Blatter, col. 4, 1. 63 to col. 5, 1. 12; see also Fig. 1, Abstract).

Appellants assert that because Dokic does not teach addressing, modifying Dokic's PID look-up tables to contain Blatter's two data structures

would defeat the purpose of limiting the capabilities of the [DSP] to interpret the data stream or provided to an external circuit by the [DSP] would defeat the purpose of limiting the capabilities of the [DSP] in order to speed up the demultiplexing, and would change the principles of operation of Dokic.

(App. Br. 24). Appellants provide no factual basis for this assertion. We agree with the Examiner's finding that the combination "use[s] known techniques to improve a similar device." (Ans. 20). *See KSR* at 1740-41.

Appellants fail to explain how employing memory addresses and two data structures in any way impedes Dokic's decoupled microprocessor architecture system. As we found above, Dokic teaches storing video, audio, and clock data in designated memory slots in the memory 205. (FF 4-7). As we also found above, this implies, at a minimum, tracking address locations of such memory 205 slots, because such information is employed by the DSP to control a switch for data processing (*see* FF 1-8).

Moreover, the Examiner found that modifying the memory with two data structures having address pointers to encryption keys and buffers as Blatter teaches (*see* FF 9) "utilizes known memory management techniques in a similar structure in order to improve Dokic by enabling it to support commonly utilizes [sic] encryption/decryption using an efficient data management method (i.e. pointers as opposed to storing multiple copies of the same information in multiple locations)." (Ans. 19). Both systems employ PID tables to demultiplex/decode MPEG data streams (FF 1-9, *see also* Ans. 9-10, 18-20). We find that the use and implementation of address pointers to another memory location/structure would have been well known (*see* FF 9, Ans. 7 – citing the 'User's Manual").

Therefore, contrary to Appellants' assertions of lack of a teaching, suggestion, and/or motivation as to how to combine the references to arrive at the claimed combination (App. Br. 23- 24, Reply Br. 3-4), we find that the

Examiner articulated, and the record supports an amply buttressed rationale under *KSR*, which Appellants have failed to rebut with sufficient evidence and/or argument. Accordingly, we will sustain the Examiner's rejection of claims 21, 29, 30 and 38, and claims 22-28 and 31-37 dependent therefrom.

35 U.S.C. § 103 rejection of claims 42 - Dokic with Bestler

Appellants submit that the Examiner has not established a prima facie case of obviousness regarding claim 42, because: "Claim 42 depends from claim 39. The Examiner does not contend...that the features of claim 39 that are missing from Dokic, as discussed above, are taught, suggested or motivated by Bestler." (Reply Br. 5). We have found *supra* that Dokic teaches all the recited limitations of claim 39. Accordingly, we will sustain the Examiner's rejection of claim 42.

CONCLUSION

We conclude that the Examiner erred in rejecting claims 11 and 13-20. Accordingly, we will not sustain the Examiner's rejections of those claims. On the other hand we have sustained the Examiner's rejections of claims 1, 3-10, 21-42, 45 and 46.

DECISION

We affirm the Examiner's decision rejecting claims 1, 3-10, 21-42, 45 and 46. We reverse the Examiner's decision rejecting claims 11 and 13-20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

gvw

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC 701 FIFTH AVE SUITE 5400 SEATTLE, WA 98104